IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). Please AMEND claims, and ADD new claims, in accordance with the following:

1. (CANCELED)

2. (CANCELED)

3. (CANCELED)

4. (CURRENTLY AMENDED) The semiconductor device according to claim 1~~8~~, wherein a thickness of each of said semiconductor elements is 50 μM or less.

5. (CURRENTLY AMENDED) The semiconductor device according to claim 1~~8~~, wherein each said semiconductor element~~s and wiring patterns corresponding thereto are~~ is electrically connected by flip chip mounting to said respective wiring pattern.

6. (CURRENTLY AMENDED) The semiconductor device according to claim 1~~8~~, wherein each said semiconductor element~~s and wiring patterns corresponding thereto are~~ is electrically connected via an anisotropically conductive film to said respective wiring pattern.

7. (CANCELED)

8. (CANCELED)

9. (CANCELED)

10. (CANCELED)

11. (CANCELED)

12. (CANCELED)

13. (CANCELED)

14. (CURRENTLY AMENDED) A semiconductor device, comprising:

a first insulating layer having vias extending therethrough;

a first conductive layer ~~having~~ , comprising a first wiring pattern, ~~s and formed~~ embedded within the first insulating layer;

a second conductive layer ~~having~~ , comprising a second wiring pattern, ~~s and~~ formed ~~over~~ on the first insulating layer, ~~one or more of~~ the wiring patterns of the second conductive layer being electrically connected to ~~one or more of~~ the wiring patterns of the first conductive layer through the vias ~~holes~~ of the first insulating layer; ~~and~~

~~at least one~~ a semiconductor element ~~imbedded within~~ embedded in the first insulating layer ~~such that the at least one semiconductor element is~~ and electrically connected to ~~at least one of~~ the wiring patterns of the first ~~conductive layer and at least one of the wiring patterns of the second~~ conductive layer; and

a second insulating layer having a semiconductor element, electrically connected to the wiring pattern of the second conductive layer, embedded therein and embedding further therein the second conductive layer.

15. (CANCELED)

16. (CURRENTLY AMENDED) The semiconductor device according to claim 14, wherein one or more of the wiring patterns of the first conductive layer is/are electrically connected to one or more of the wiring patterns of the second conductive layer through corresponding said vias.

17. (CURRENTLY AMENDED) A semiconductor device, comprising:

a substrate;

a first set of conductors ~~within~~ comprising a first conductive layer formed on the substrate;

a first insulating layer formed ~~over~~ on the first set of conductors and having vias extending therethrough, the first insulating layer having at least one semiconductor element and the first set of conductors embedded therein;

a second set of conductors ~~within~~ comprising a second conductive layer formed ~~above~~ on the first insulating layer and extending through vias therein; and

a second insulating layer formed ~~over~~ on the second set of conductors and having vias extending therethrough, the second insulating layer having at least one semiconductor element and portions of the second set of conductors ~~imbedded~~ embedded therein;

wherein one or more of the first set of conductors ~~and one or more of the second set of conductors are~~ is/are electrically connected to the at least one semiconductor element ~~imbedded~~ embedded in the first insulating layer and through corresponding said vias to one or more of the second set of conductors and one or more of the second set of conductors is/are electrically connected to the at least one semiconductor element ~~imbedded~~ embedded in the second insulating layer and through corresponding said vias to one or more of the first set of conductors.

18. (NEW) A semiconductor device, comprising:

a substrate having a main surface;

plural device layers stacked, in succession, on the main surface of the substrate, each device layer comprising:

a conductive layer comprising a wiring pattern,

a semiconductor element electrically connected to the wiring pattern, and

a single insulating layer respectively associated with and embedding therein the semiconductor element and the respective conductor layer having conductive vias extending therethrough, and

the wiring pattern of the conductive layer of each successive, stacked device layer being formed on an upper main surface of the single insulating layer of the respective, underlying device layer and respective said wiring patterns of the conductive layers of the plural stacked device layers being selectively electrically interconnected through the corresponding vias of the respective, single insulating layers of the stacked, plural device layers.

19. (NEW) The semiconductor device according to claim 18, wherein:

the semiconductor elements are commonly disposed within the respective insulating

layers and aligned in the plural, stacked device layers.

20. (NEW) The semiconductor device according to claim 18, further comprising:

plural semiconductor elements in each of the plural device layers and commonly disposed therein so as to be in aligned relationship in the stacked layers.

21. (NEW) The semiconductor device according to claim 18, wherein each insulating layer surrounds and covers substantially all of each outer surface of the semiconductor element embedded therein.